
PULSE WIDTH MODULATION AMPLIFIERS

FEATURES

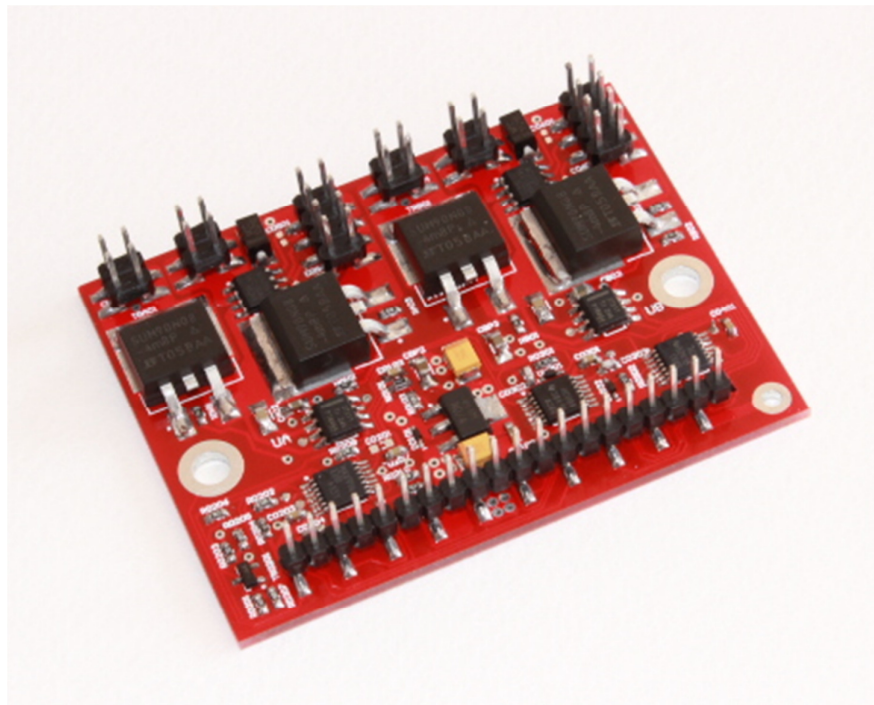
- CONSTRUCTED ON MCPCB(Metal Core PCB)
- LOW THERMAL RESISTANCE
- LOW COST
- HIGH VOLTAGE – 100 VOLTS
- HIGH CURRENT- 180 AMPS
- HIGH EFFICIENCY
- HIGH FREQUENCY – 250KHz
- LOW BRIDGE RESISTANCE-8mohm max
- 18kW OUTPUT CAPABILITY
- DEAD TIME CONTROLLER
- VARIABLE SWITCHING FREQUENCY

APPLICATIONS

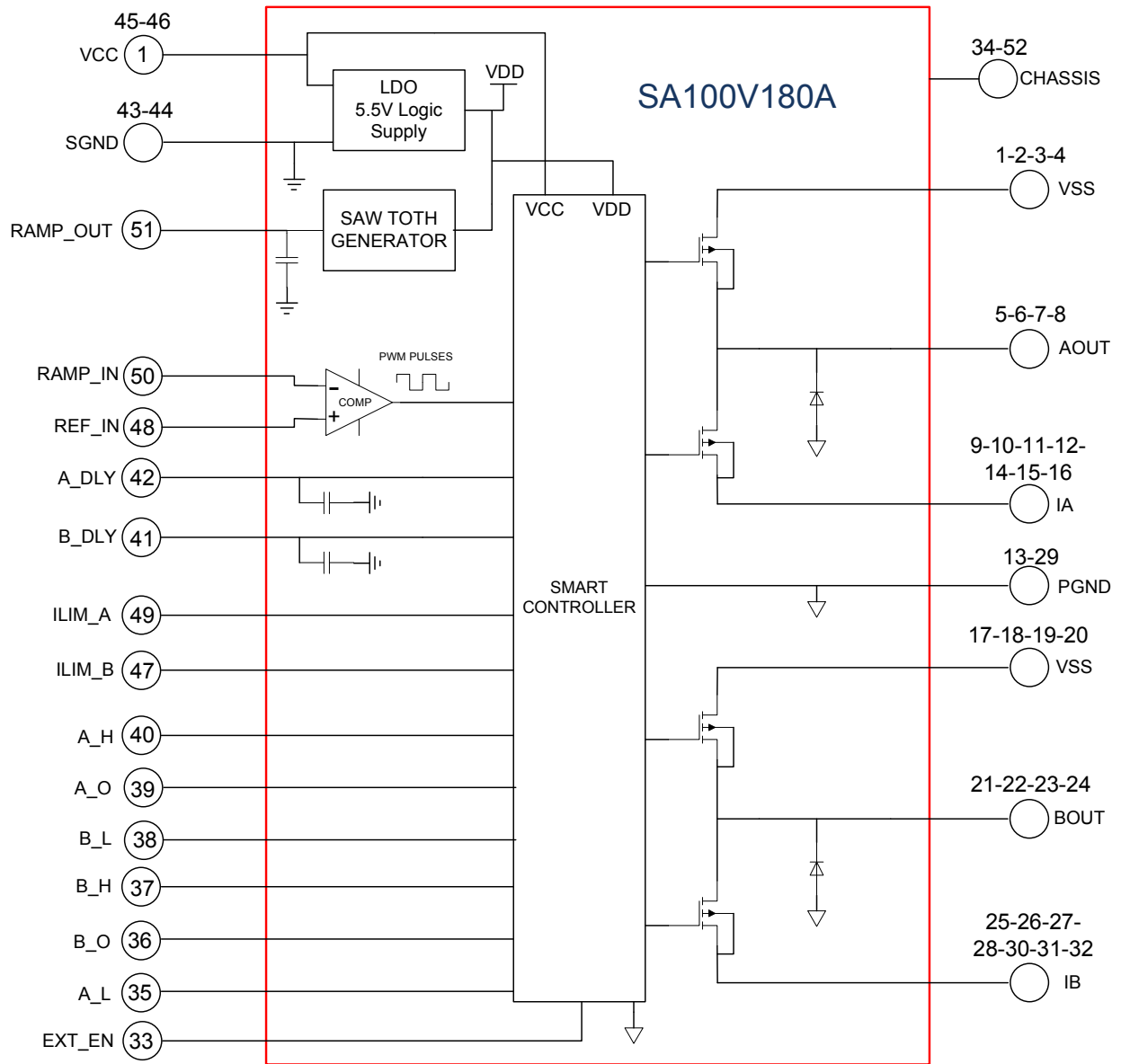
- CLASS D SWITCHING AMPLIFIER
- LASER DIODE DRIVER
- BRUSH MOTOR CONTROL
- MRI
- TEC CONTROL
- MAGNETIC BEARING

DESCRIPTION

The SA100V180A is a PWM amplifier that constructed on MCPCB (Metal Core PCB). This provides cost effective, high efficient and low thermal resistance solution in many industrial applications. The SA100V180A offers outstanding performance that rivals many much more expensive hybrid components. The SA100V180A is a complete PWM amplifier including an frequency adjustable saw tooth generator , comparator, current limit comparators, adjustable dead time control, integrated smart H-Bridge controller and a full H-Bridge output circuit has output impedance as low as 8mohm. These features provide to drive high power loads up to 18kW at 25°C case temperature. The SA100V180A can be used for driving weaker load in higher temperature environments. The module has efficiency as high as 97% at full load and has thermal resistance as low as 1.2°C/W. The bottom side of module is component side and upper side of the module is full metal plate to drain heat load from module easily. These superior performances make this module a proper solution for high temperature applications.



EQUIVALENT CIRCUIT DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, VSS	100V
SUPPLY VOLTAGE, VCC	20V
OUTPUT CURRENT, peak	180A, within SOA
POWER DISSIPATION, internal, DC	600W ³
SIGNAL INPUT VOLTAGES	5.5V
TEMPERATURE, pin solder, 10s	225°C
TEMPERATURE, junction ²	175°C
TEMPERATURE RANGE, storage	-40°C to 105°C
OPERATING TEMPERATURE, case	-40°C to 85°C

SPECIFICATIONS

PARAMETERS	TEST CONDITIONS ¹	MIN	TYP	MAX	UNITS
SAW TOOTH GENERATOR RAMP_OUT					
HIGH LEVEL VOLTAGE	Full temperature range	3.4	3.5	3.6	V
LOW LEVEL VOLTAGE	Full temperature range	0.3	0.4	0.5	V
FREQUENCY	No external cap on RAMP_OUT Pin	240	250	260	KHz
DEAD TIME CONTROL					
ON Delay upper to lower MOSFETs	No external cap on A_DLY&B_DLY Pin	150	160	-	ns
OFF Delay upper to lower MOSFETs		150	160	-	ns
OUTPUT					
TOTAL R _{ON} , both MOSFETs ⁴	I _o =180A, T _j =85°C	8	9	10	mΩ
CURRENT, continuous				180	A
CURRENT, peak	100ms			200	A
OUTPUT MOSFET BODY DIODE					
CONTINUOUS CURRENT					
FORWARD VOLTAGE	I= 110A			1.3	V
REVERSE RECOVERY	I _r =110A			60	ns
POWER SUPPLY					
VOLTAGE, VS		3	60	100	V
VOLTAGE, VCC		8	12	17	V
VOLTAGE, VDD		5.4	5.5	5.6	V
CURRENT, VS, quiescent	20kHz Switching		4	28	mA
CURRENT, VCC, quiescent	20kHz Switching			18	mA
CURRENT, VCC, shutdown				12	mA
THERMAL					
RESISTANCE, DC, junction to case	Full temperature range			1.2	°C/W
RESISTANCE, junction to air	Full temperature range			14	°C/W
TEMPERATURE RANGE, case		-40		85	°C

NOTES:

1. Unless otherwise noted: T_c=25°C, V_{cc}= 15V, V_s=60V
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.
3. Each of the two output transistors on at any one time can dissipate 150W.
4. Maximum specification guaranteed but not tested.

SPECIFICATIONS CONTINUED

PARAMETERS	TEST CONDITIONS ¹	MIN	TYP	MAX	UNITS
AH_IN, AL_IN, BH_IN, BL_IN ,EXT_EN INPUTS					
VHIT, High Input Voltage Threshold	Full temperature range	1.9	2.3	2.7	V
VLIT, Low Input Voltage Threshold	Full temperature range	1.3	1.6	1.9	V
A_O, B_O OUTPUTS					
VOH, High Level Output Voltage	Full temperature range	5.3	5.35	5.4	V
VOL, Low Level Output Voltage	Full temperature range	0.2	0.3	0.4	V
ILIM_A, ILIM_B INPUTS					
INPUT VOLTAGE LEVEL		-0.3		5.5	V
Current Protect Voltage Threshold		170	180	185	mV
RAMP_IN INPUTS					
INPUT VOLTAGE LEVEL		-0.3	-	5.5	V

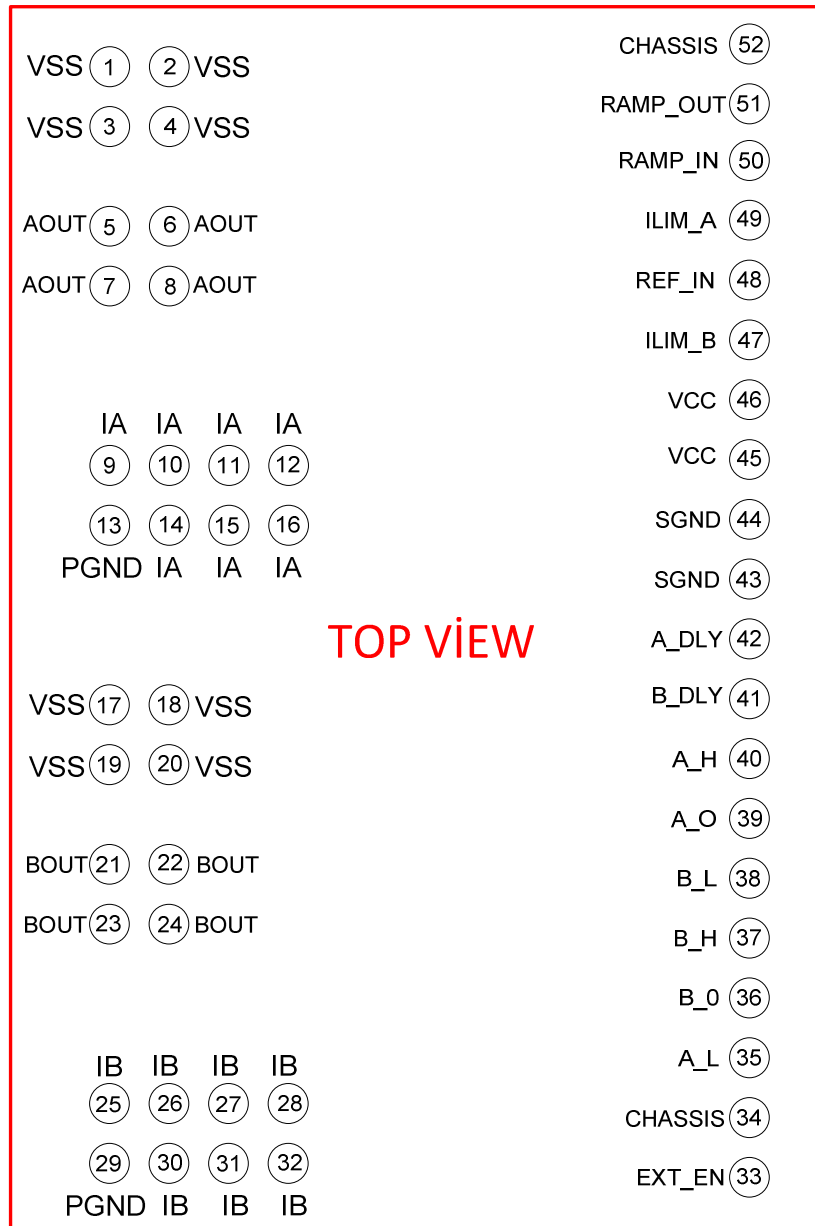


Figure 1 PIN CONFIGURATION

PIN FUNCTIONS

PIN NAME	PIN NO	I/O	DESCRIPTION
VSS	1, 2, 3, 4, 17, 18, 19, 20	-	Load Supply Pin. Decouple this pin to PGND with tantalum or electrolytic capacitor of at least 10 μ F per output ampere to drive load. In addition place ceramic capacitor 1 μ F or greater directly at each set of pins for high frequency bypassing. Bypass capacitors to Load Supply terminals VSS must be connected physically close to the pins to prevent local parasitic oscillation and overshoot.
AOUT	5, 6, 7, 8	-	Half Bridge A output
IA	9, 10, 11, 12, 14, 15, 16	-	Return path for Half Bridge A. This pin can be connected directly to PGND or can be connected to current sense resistor for current measuring.
PGND	13, 29	-	Load Supply (VSS) return Pin.
BOUT	21, 22, 23, 24	-	Half Bridge B output
IB	25, 26, 27, 28, 30, 31, 32	-	Return path for Half Bridge B. This pin can be connected directly to PGND or can be connected to current sense resistor for current measuring.
EXT_EN	33	I	External Enable Input. When logic HIGH all driver outputs AOUT and BOUT are active when logic LOW all driver outputs are high impedance state.
CHASSIS	34, 52	-	These pins are connected to aluminum back plate. To increase EMI ,EMC performance connect these pins to SGND pin via ceramic capacitor bigger than 10 μ F.
A_L	35	I	Logic control input for low side Mosfet of Half Bridge A
B_O	36	O	Logic control output to drive A_L and B_H control inputs. If H bridge will not be controlled individually for each logic inputs from external H Bridge logic controller, this pin should be connected to A_L and B_H control inputs.
B_H	37	I	Logic control input for high side Mosfet of Half Bridge B
B_L	38	I	Logic control input for low side Mosfet of Half Bridge B
A_O	39	O	Logic control output to drive B_L and A_H control inputs. If H bridge will not be controlled individually for each logic inputs from external H Bridge logic controller, this pin should be connected to B_L and A_H control inputs.
A_H	40	I	Logic control input for high side Mosfet of Half Bridge A
B_DLY	41	O	Dead time adjustment pin between upper and lower MOSFETs of Half Bridge B. If 100ns dead time is enough this pin should be no connection.
A_DLY	42	O	Dead time adjustment pin between upper and lower MOSFETs of Half Bridge A. If 100ns dead time is enough this pin should be no connection
SGND	43, 44	-	Signal ground for low noise analog circuit and logic controller inside module. For proper operation during PCB layout the PGND signal should be connected to this pin via trace, and CHASSIS pin should be connected to this pin via ceramic capacitor bigger than 10 μ F

PIN NAME	PIN NO	I/O	DESCRIPTION
VCC	45, 46	-	Supply voltage for low noise analog circuits and logic controllers. Decouple this pin to SGND with ceramic capacitor bigger than 10 μ F. Bypass capacitors to terminal VCC must be connected physically close to the pins to prevent local parasitic oscillation and overshoot.
ILIM_B	47	I	Current sense comparator input for Half Bridge B. If current sense comparator will not be used this pin should be connected to PGND signal.
REF_IN	48	I	
ILIM_A	49	I	Current sense comparator input for Half Bridge A. If current sense comparator will not be used this pin should be connected to PGND signal.
RAMP_IN	50	I	Ramp input of PWM comparator inside module. If the saw tooth generator of comparator will be used the RAMP_OUT pin of module should be connected to this pin.
RAMP_OUT	51	O	Saw tooth generator output pin of the module.

TYPICAL APPLICATION

With the addition of a few external components the SA100V180A becomes a motor torque controller. In the SA100V180A the source terminal of each low side MOSFET driver is brought out for current sensing via R_SA and R_SB. A2 is use as an error amplifier for current loop control. A1 is a differential amplifier that amplifies the difference in currents of the two half bridges. This signal is fed into the A2 error amplifier that mixes the current signal and the control signal. The output of A2 is an input signal to the SA100V180A that controls the torque on the motor.

SAW TOOTH GENERATOR

The SA100V180A includes a user frequency programmable saw tooth generator (STG). STG is connected to RAMP_OUT pin of the module. The STG determines the switching frequency of the amplifier. The frequency of the STG can be prograded by connecting proper capacitor to RAMP_OUT pin of the amplifier. There is a default internally 1nF capacitor connected to this pin provides maximum 260KHz switching frequency for high frequency PWM application like driving DC load that needs minimum valued output filter component. If user need to lower the frequency, by connecting proper capacitance to RAMP_OUT pin the frequency can be adjusted. The frequency of PWM amplifier according to external capacitance value is determined by given Formula:

Rise time of STG, $T_r = 1.17 \times 1500 \times (1nF + C_{ext})$
 Fall time of STG, $T_f = 2.7 \times 1000 \times (1nF + C_{ext})$
 Frequency of STG $f = 1 / (T_r + T_f)$

Also note that to drop frequency will cause to drop peak to peak value of saw tooth waveform. For instance if 100nF external capacitor connected, the frequency will drop to 2.9kHz and saw tooth wave form peaks will be at 3.28V and 0.36V.

The RAMP_IN input pin on SA100V180A is the STG input pin of PWM comparator which placed inside the module. The own STG of SA100V180A or RAMP_OUT pin can be connected to RAMP_IN pin. But if user wants to use external STG, user can connect external STG to RAMP_IN pin unless the signal specifications are out of the module limits.

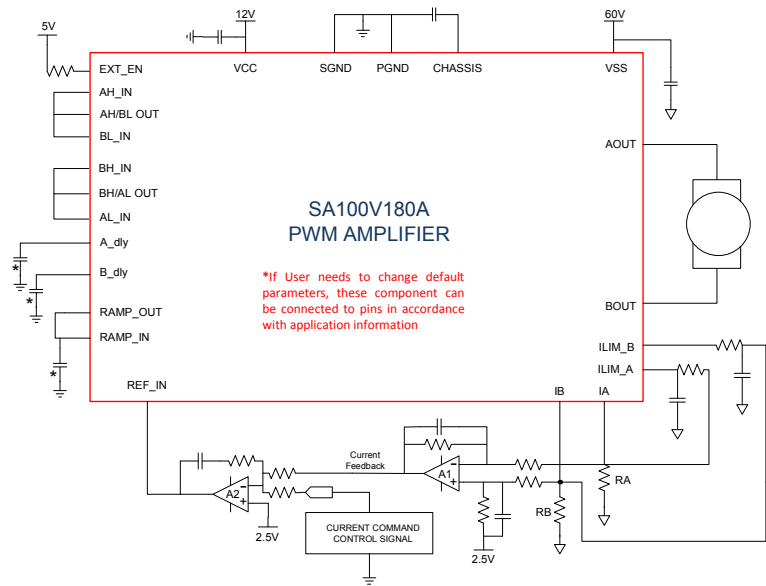


Figure 2 TORQUE MOTOR CONTROL

SHUTDOWN

The SA100V180A output stage can be turned off with shutdown command voltage applied to EXT_EN pin. In case of LOW signal in this pin will disable to module output and output stage will be in high impedance state.

Other way to turn off module is to apply more than 180mV input signal to ILIM_A and ILIM_B pins of the module. These pins are designed to provide over current protection on module. So in case of EXT_EN signal is LOW or any one of the ILIM_A or ILIM_B pin signals are more than 180mV the module will turned off .

CURRENT SENSING

The low side drive MOSFETs of the SA100V180A are brought out for sensing the current in each half bridge. A resistor from each sense line to PGND develops the current sense voltage.. Choose R and C such that the time constant is equal to 10 periods of the selected switching frequency. The internal current limit comparators trips at 180mV. Therefore, current limit occurs at $I = 0.18V / R_{sense}$ for each half bridge. See Figure3. Accurate milliohm power resistors are required for proper operation.

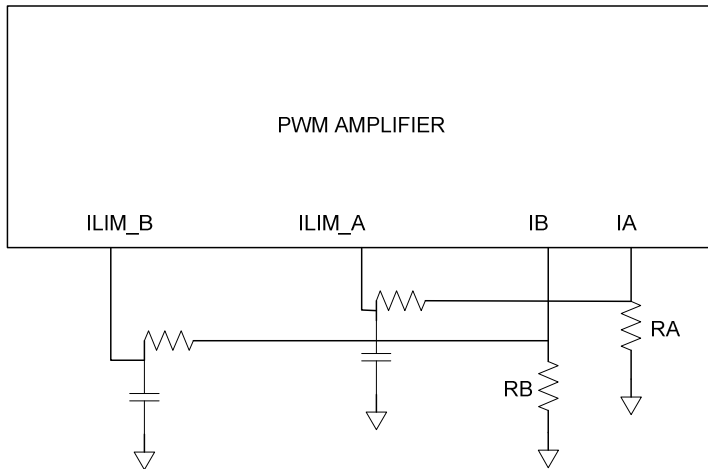


Figure 3 CURRENT SENSING CIRCUIT

POWER SUPPLY BYPASSING

Bypass capacitors to Supply terminals VSS and VCC must be connected physically close to the pins to prevent local parasitic oscillation and overshoot. All VSS pins must be connected together. Place an tantalum or electrolytic capacitor of at least 10 μ F per output ampere to drive load. In addition place ceramic capacitor 1 μ F or greater directly at each set of pins for high frequency bypassing.

GROUNDING AND PCB LAYOUT

Switching amplifiers combine millivolt level analog signals and large amplitude switching voltages and currents with fast rise times. As such grounding is crucial. Use a single point ground at SGND (pins 43 and 44). Connect PGND signal to SGND terminal. Connect Chassis signal to SGND pin via ceramic capacitor bigger than 10 μ . Connect the ground terminal of the VCC supply directly to SGND as well. Make sure no current from the load return to PGND flows in the analog signal ground. Make sure that the power portion of the PCB layout does not pass over low level analog signal traces on the opposite side of the PCB. Capacitive coupling through the PCB may inject switching voltages into analog signal path. Further, make sure that the power side of the PCB layout does not come close to the analog signal side. Fast rising output signal can couple through the trace-to-trace capacitance on the same side of the PCB.

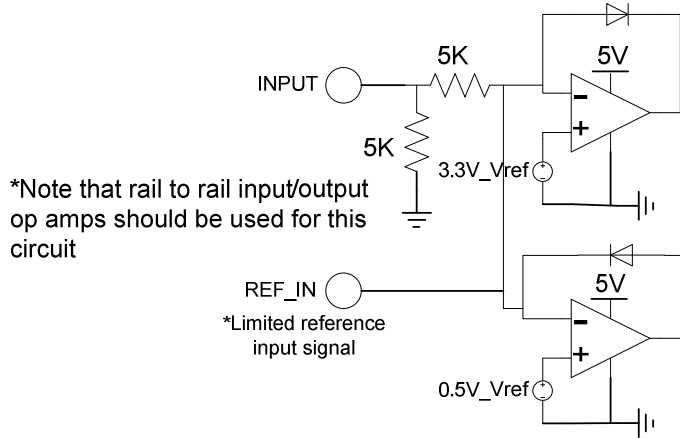
DEAD TIME ADJUSTMENT

The SA100V180A has already dead time controller inside the module. These dead time controller circuits provide approximately 160ns dead time duration between upper and lower MOSFETs of each Half Bridge. If user needs to increase the dead time duration, capacitive load connection pins of the dead time controller circuits for each Half Bridge are brought out of the module via A_DLY and B_DLY pins. By connecting extra capacitor to these pins will increase the dead time duration. To increase dead time duration for every Nano second one Pico farad capacitor should be connected to these pins. If 160ns dead time is enough these pins should have no connection.

DETERMINING THE OUTPUT STATE

The input signal is applied to REF_IN (Pin 28) and varies from 0.3 to 3.5 volts, zero to full scale. As REF_IN varies from 0.3 to 2 volts the B output “high” duty cycle (relative to ground) is greater than the A output “high” duty cycle. The reverse occurs as the input signal varies from 2 to 3.5 volts. When REF_IN = 2 volts the duty cycles of both A and B outputs are 50%. Consequently when the input voltage is 3.5V the A output is close to 100% duty cycle and the B output is close to 0% duty cycle. The reverse occurs with an input voltage of 0.3V. The output duty cycle extremes vary somewhat with switching frequency.

If REF_IN signals exceeds the lower and upper limits of the saw tooth signals the output of the PWM amplifier enters “lock out” state. Because 100% and 0% duty cycle is not supported from any high power H Bridge topologies. The charge pump circuits of high side MOSFET driver circuits needs toggling control signal inputs to be able to work properly. So to prevent PWM amplifier from lock out state simple input signal limiter circuit can be implemented by few components. The input limiter circuit shown in Figure 4 can be used.



*Note that rail to rail input/output op amps should be used for this circuit

APPLICATION WITH MCU

This module is designed to be used with MCU (Micro Controller Unit). If user wants to use this module with MCU instead of analog controlled loop, this module can be adapted easily to digital platform. Figure 5 shows typical application of SA100V180A that used with MCU.

Figure 4 VOLTAGE LIMITER CIRCUIT

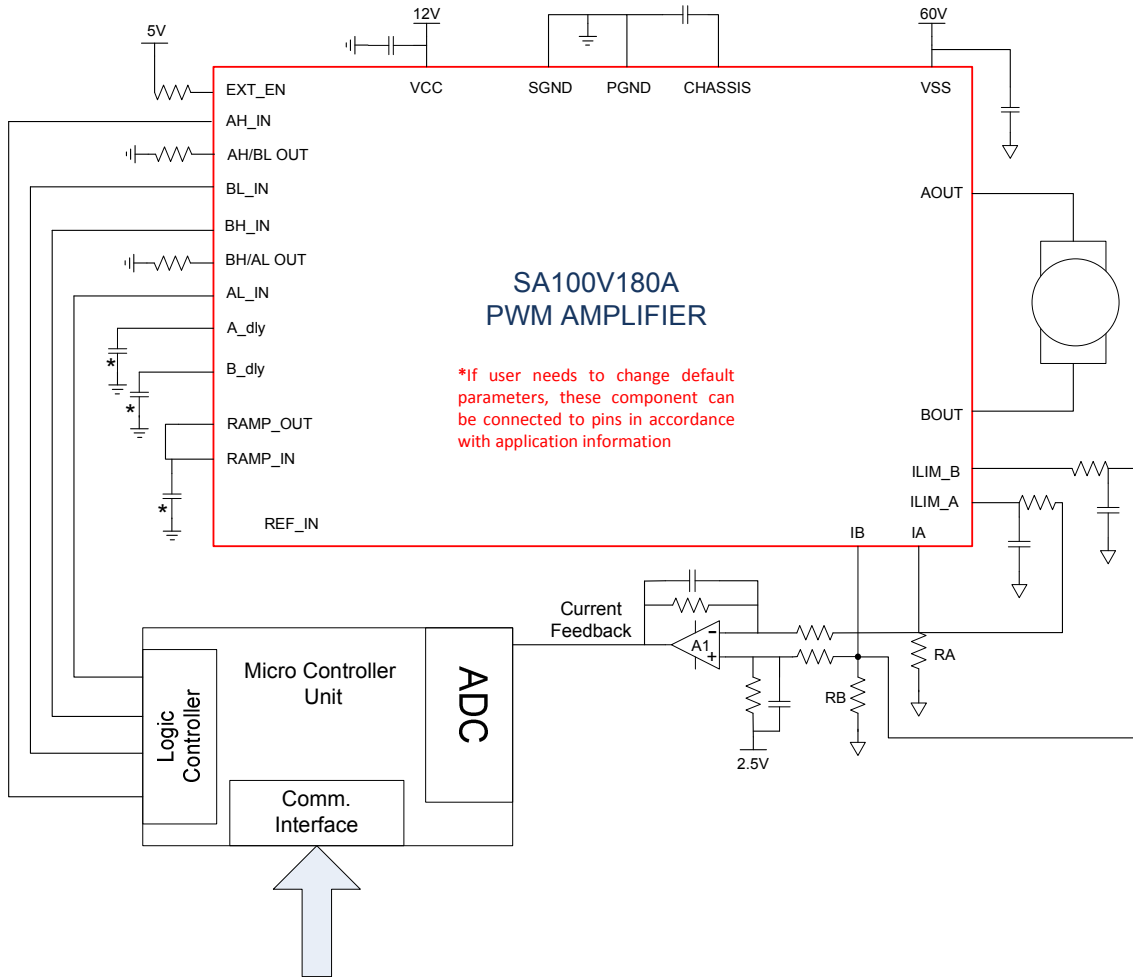


Figure 5 MCU APPLICATIONS WITH SA100V180A

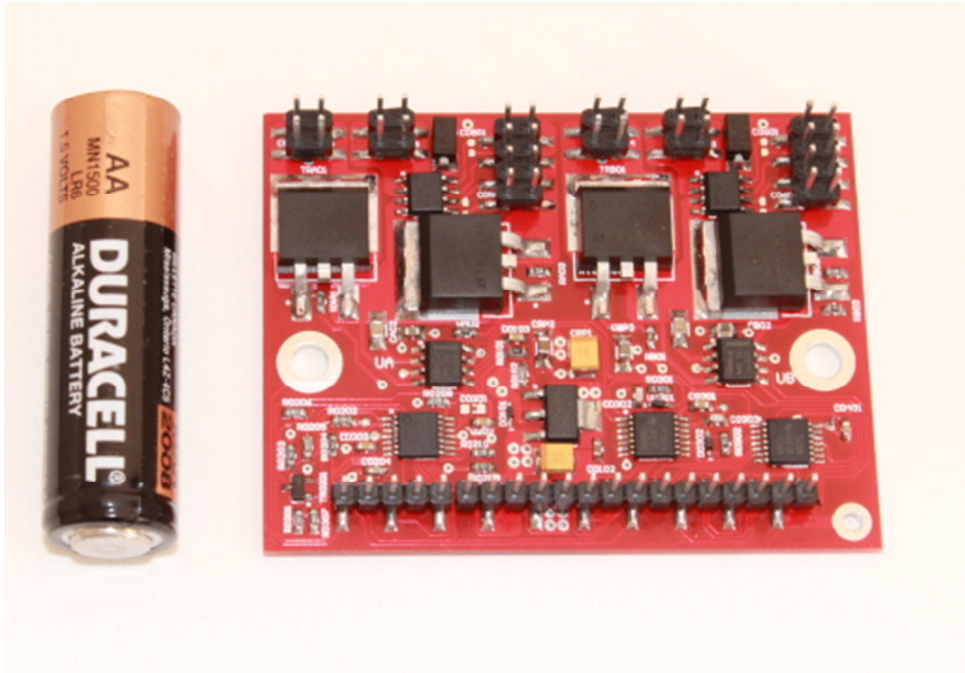


Figure 6 BOTTOM VIEW OF SA100V180A

